AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A programmable logic device comprising:

programmable input/output circuitry;

programmable core logic coupled to the programmable input/output circuitry;

a multi-gigabit transceiver coupled to the programmable core logic;

a first pair of clock pads; ~~and~~

a dedicated routing structure directly connecting the first pair of clock pads and the multi-gigabit transceiver~~.~~; and

a down-level shifter connected to the dedicated routing structure.

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2. (Original) The programmable logic device of Claim 1, wherein the dedicated routing structure comprises:

a differential buffer coupled to the first pair of clock pads; and

a first clock trace providing a direct connection between the differential buffer and the multi-gigabit transceiver.

3. (Original) The programmable logic device of Claim 1, further comprising:

a second pair of clock pads; and

a second dedicated routing structure directly connecting the second pair of clock pads and the multi-gigabit transceiver.

4. (Original) The programmable logic device of Claim 3, wherein the second dedicated routing structure comprises:

a second differential buffer coupled to the second pair of clock pads; and

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a second clock trace providing a direct connection between the second differential buffer and the multi-gigabit transceiver.

5. (Original) The programmable logic device of Claim 4, further comprising a first multiplexer coupled to the first and second clock traces, the first multiplexer being configured to selectively route a clock signal on either the first or second clock trace in response to a select signal.

6. (Original) The programmable logic device of Claim 5, further comprising a programmable connection between the programmable core logic and the first multiplexer, wherein the programmable core logic provides the select signal to the first multiplexer.

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7. (Original) The programmable logic device of Claim 5, wherein the first multiplexer comprises:

a first transmission gate configured to be enabled in response to the select signal;

a second transmission gate configured to be enabled in response to the inverse of the select signal;

a first logic gate having input terminals coupled to receive a clock signal on the dedicated routing structure and the select signal, and an output terminal coupled to the first transmission gate; and

a second logic gate having input terminals coupled to receive a clock signal on the second clock trace and the inverse of the select signal, and an output terminal coupled to the second transmission gate.

8. (Original) The programmable logic device of Claim 5, wherein the multi-gigabit transceiver comprises a phase locked loop configured to receive the clock signal selected by the first multiplexer.

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9. (Original) The programmable logic device of Claim 8, wherein the multi-gigabit transceiver further comprises a serializer configured to operate in response to a serializing clock signal generated by the phase locked loop in response to the clock signal selected by the first multiplexer.

10. (Original) The programmable logic device of Claim 1, further comprising:

a first general-purpose clock pad;

a first down-level shifter coupled to the first general-purpose clock pad; and

a general-purpose clock routing path coupling the down-level shifter to the multi-gigabit transceiver.

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11. (Original) The programmable logic device of Claim 10, further comprising a multiplexer coupled to the dedicated routing structure and the general-purpose clock routing path, the multiplexer being configured to selectively route a clock signal on either the dedicated routing structure or the general-purpose clock routing path in response to a select signal.

12. (Original) The programmable logic device of Claim 11, further comprising a first configuration memory cell that is programmable to store and provide the select signal.

13. (Original) The programmable logic device of Claim 11, wherein the multiplexer comprises:

a first transmission gate configured to be enabled in response to the select signal;

a second transmission gate configured to be enabled in response to the inverse of the select signal;

a first logic gate having input terminals coupled to receive a clock signal on the dedicated routing structure and the select signal, and an output terminal coupled to the first transmission gate; and

a second logic gate having input terminals coupled to

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receive a clock signal on the general-purpose clock routing path and the inverse of the select signal, and an output terminal coupled to the second transmission gate.

14. (Original) The programmable logic device of Claim 11, wherein the multi-gigabit transceiver comprises a phase locked loop configured to receive the clock signal selected by the multiplexer.

15. (Original) The programmable logic device of Claim 14, wherein the multi-gigabit transceiver further comprises a serializer configured to operate in response to a serializing clock signal generated by the phase locked loop in response to the clock signal selected by the multiplexer.

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16. (Original) The programmable logic device of Claim 1, wherein the multi-gigabit transceiver comprises a physical media access (PMA) sublayer and a physical coding sublayer (PCS).

17. (Original) The programmable logic device of Claim 16, further comprising means for routing a clock signal on the dedicated routing structure to a phase locked loop in the PMA as a PMA reference clock signal.

18. (Original) The programmable logic device of Claim 17, further comprising a down-level shifter configured to receive the PMA reference clock signal, and in response, provide a PCS reference clock signal to the PCS.

19. (Original) The programmable logic device of Claim 1, wherein the first pair of clock pads is located near the center of an edge of the programmable logic device.

20. (Currently Amended) A method of operating a programmable logic device, the method comprising:

applying a first clock signal to a first pair of clock

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pads of the programmable logic device;

routing the first clock signal on dedicated routing resources from the first pair of clock pads to a multi-gigabit transceiver located on the programmable logic device; ~~and~~

using the first clock signal to control the multi-gigabit transceiver;

applying a second clock signal to a general-purpose clock pad of the programmable logic device;

routing the second clock signal from the general-purpose clock pad through clock routing resources of the programmable logic device to the multi-gigabit transceiver; and

selecting either the first clock signal or the second clock signal to control the multi-gigabit transceiver.

21. (Original) The method of Claim 20, wherein the first clock signal is a differential clock signal at the first pair of clock pads.

22. (Original) The method of Claim 21, wherein the first clock signal exhibits jitter of less than 40 picoseconds peak-to-peak.

23. (Original) The method of Claim 20, further comprising:

operating core logic of the programmable logic device in response to a core voltage supply;

operating an I/O region of the programmable logic device in response to an I/O voltage supply, wherein the I/O voltage supply is greater than the core voltage supply; and

routing the first clock signal at a signaling level corresponding with the I/O voltage supply.

Claims 24-26 Cancelled.

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27. (Currently Amended) The method of Claim ~~26~~20, further comprising:

programming a configuration memory cell of the programmable logic device to store a select value; and

selecting either the first clock signal or the second clock signal in response to the select value.

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28. (Currently Amended) The method of Claim ~~26~~20, wherein the second clock signal is a single-ended clock signal.

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29. (Original) The method of Claim 20, further comprising routing the first clock signal to a phase locked loop in a physical media access (PMA) sublayer of the multi-gigabit transceiver as a PMA reference clock signal.

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30. (Original) The method of Claim ~~29~~, further comprising converting the PMA reference clock signal to a lower voltage signal for use in a physical coding sublayer (PCS) of the multi-gigabit transceiver.

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31. (Currently Amended) A programmable logic device comprising:

means for applying a first clock signal to a first pair of clock pads of the programmable logic device;

dedicated means for routing the first clock signal from the first clock pad to a multi-gigabit transceiver located on the programmable logic device; ~~and~~

means for using the first clock signal to control the multi-gigabit transceiver;

means for applying a second clock signal to a general-purpose clock pad of the programmable logic device;

means for routing the second clock signal from the general-purpose clock pad through clock routing resources of the programmable logic device to the multi-gigabit transceiver; and

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means for selecting either the first clock signal or the second clock signal to control the multi-gigabit transceiver.

32. (Original) The programmable logic device of Claim 31, wherein the first clock signal is a differential clock signal at the first clock pad.

33. (Original) The programmable logic device of Claim 32, wherein the first clock signal exhibits jitter of less than 40 picoseconds peak-to-peak.

34. (Original) The programmable logic device of Claim 31, further comprising:

means for operating core logic of the programmable logic device in response to a core voltage supply;

means for operating an I/O region of the programmable logic device in response to an I/O voltage supply, wherein the I/O voltage supply is greater than the core voltage supply; and

means for routing the first clock signal at a signaling level corresponding with the I/O voltage supply.

Claims 35-37 Cancelled.

38. (Currently Amended) The programmable logic device of Claim ~~37~~31, further comprising:

means for programming a configuration memory cell of the programmable logic device to store a select value; and

means for selecting either the first clock signal or the second clock signal in response to the select value.

39. (Currently Amended) The programmable logic device of Claim ~~37~~31, wherein the second clock signal is a single-ended clock signal.

34 40. (Original) The programmable logic device of Claim 28, further comprising means for routing the first clock signal to a phase locked loop in a physical media access (PMA) sublayer of the multi-gigabit transceiver as a PMA reference clock signal.

35 41. (Previously Amended) The programmable logic device of Claim 34, further comprising means for converting the PMA reference clock signal to a lower voltage signal for use in a physical coding sublayer of the multi-gigabit transceiver.

36 42. (Currently Amended) A system, comprising:

a programmable logic device including:

programmable input/output circuitry,

programmable core logic coupled to the programmable input/output circuitry,

a multi-gigabit transceiver coupled to the programmable core logic,

a first pair of clock pads, and

a dedicated routing structure ~~directly~~ connecting the first pair of clock pads and the multi-gigabit transceiver via a first multiplexer, wherein the first multiplexer comprises:

a first transmission gate configured to be enabled in response to a select signal;

a second transmission gate configured to be enabled in response to the inverse of the select signal;

a first logic gate having input terminals coupled to receive a clock signal on the dedicated routing structure and the select signal, and an output terminal coupled to the first transmission gate; and

a second logic gate having input terminals coupled to receive a clock signal on the second clock trace and the inverse of the select signal, and an output terminal coupled to the second transmission gate.; ~~and~~

~~a clock generation circuit coupled to the first pair of clock pads.~~

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43. (Currently Amended) The system of Claim 42, wherein the dedicated routing structure comprises:

a differential buffer coupled to the first pair of clock pads; and

a first clock trace providing a ~~direct~~ connection between the differential buffer and the multi-gigabit transceiver.

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44. (Currently Amended) The system of Claim 42, wherein the programmable logic device further comprises:

a second pair of clock pads; and

a second dedicated routing structure ~~directly~~ connecting the second pair of clock pads and the multi-gigabit transceiver.

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45. (Currently Amended) The system of Claim 44, wherein the second dedicated routing structure comprises:

a second differential buffer coupled to the second pair of clock pads; and

a second clock trace providing a ~~direct~~ connection between the second differential buffer and the multi-gigabit transceiver.

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46. (Currently Amended) The system of Claim 45, wherein the ~~programmable logic device further comprises a~~ first multiplexer is coupled to the first and second clock traces, the first multiplexer being configured to selectively route a clock signal on either the first or second clock trace in response to a select signal.

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47. (Previously Added) The system of Claim 46, wherein the programmable logic device further comprises a programmable connection between the programmable core logic and the first multiplexer, wherein the programmable core logic provides the

select signal to the first multiplexer.

Claim 48 Cancelled.

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49. (Previously Added) The system of Claim 48, wherein the multi-gigabit transceiver comprises a phase locked loop configured to receive the clock signal selected by the first multiplexer.

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50. (Previously Added) The system of Claim 49, wherein the multi-gigabit transceiver further comprises a serializer configured to operate in response to a serializing clock signal generated by the phase locked loop in response to the clock signal selected by the first multiplexer.

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51. (Previously Added) The system of Claim 42, wherein the programmable logic device further comprises:

a first general-purpose clock pad;

a first down-level shifter coupled to the first general-purpose clock pad; and

a general-purpose clock routing path coupling the down-level shifter to the multi-gigabit transceiver.

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52. (Previously Added) The system of Claim 51, wherein the programmable logic device further comprises a multiplexer coupled to the dedicated routing structure and the general-purpose clock routing path, the multiplexer being configured to selectively route a clock signal on either the dedicated routing structure or the general-purpose clock routing path in response to a select signal.

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53. (Previously Added) The system of Claim 52, wherein the programmable logic device further comprises a first configuration memory cell that is programmable to store and provide the select signal.

54. (Previously Added) The system of Claim 52, wherein the multiplexer comprises:

a first transmission gate configured to be enabled in response to the select signal;

a second transmission gate configured to be enabled in response to the inverse of the select signal;

a first logic gate having input terminals coupled to receive a clock signal on the dedicated routing structure and the select signal, and an output terminal coupled to the first transmission gate; and

a second logic gate having input terminals coupled to receive a clock signal on the general-purpose clock routing path and the inverse of the select signal, and an output terminal coupled to the second transmission gate.

55. (Previously Added) The system of Claim 52, wherein the multi-gigabit transceiver comprises a phase locked loop configured to receive the clock signal selected by the multiplexer.

56. (Previously Added) The system of Claim 55, wherein the multi-gigabit transceiver further comprises a serializer configured to operate in response to a serializing clock signal generated by the phase locked loop in response to the clock signal selected by the multiplexer.

57. (Previously Added) The system of Claim 42, wherein the multi-gigabit transceiver comprises a physical media access (PMA) sublayer and a physical coding sublayer (PCS).

58. (Previously Added) The system of Claim 57, wherein the programmable logic device further comprises means for routing a clock signal on the dedicated routing structure to a phase locked loop in the PMA as a PMA reference clock signal.

59. (Previously Added) The system of Claim 58, wherein

the programmable logic device further comprises a down-level shifter configured to receive the PMA reference clock signal, and in response, provide a PCS reference clock signal to the PCS.

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60. (Previously Added) The system of Claim 42, wherein the first pair of clock pads is located near the center of an edge of the programmable logic device.

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61. (New) A method of operating a programmable logic device, the method comprising:

applying a first clock signal to a first pair of clock pads of the programmable logic device;

applying a second clock signal to a second pair of clock pads of the programmable logic device; and

selectively routing on dedicated routing resources either the first clock signal from the first pair of clock pads or the second clock signal from the second pair of clock pads to a phase locked loop of a multi-gigabit transceiver located on the programmable logic device.

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62. (New) The method of Claim 61, further comprising:

providing a select value from programmable core logic of the programmable logic device; and

selecting the first clock signal or the second clock signal in response to the select value.

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63. (New) The method of Claim 61, wherein the second pair of clock pads comprises general-purpose clock pads of the programmable logic device.

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64. (New) The method of Claim 61, further comprising:

programming a configuration memory cell of the programmable logic device to store a select value; and

selecting either the first clock signal or the second clock signal in response to the select value.

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58 ~~65~~. (New) The method of Claim 57 ~~64~~, wherein the second clock signal is a single-ended clock signal.

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